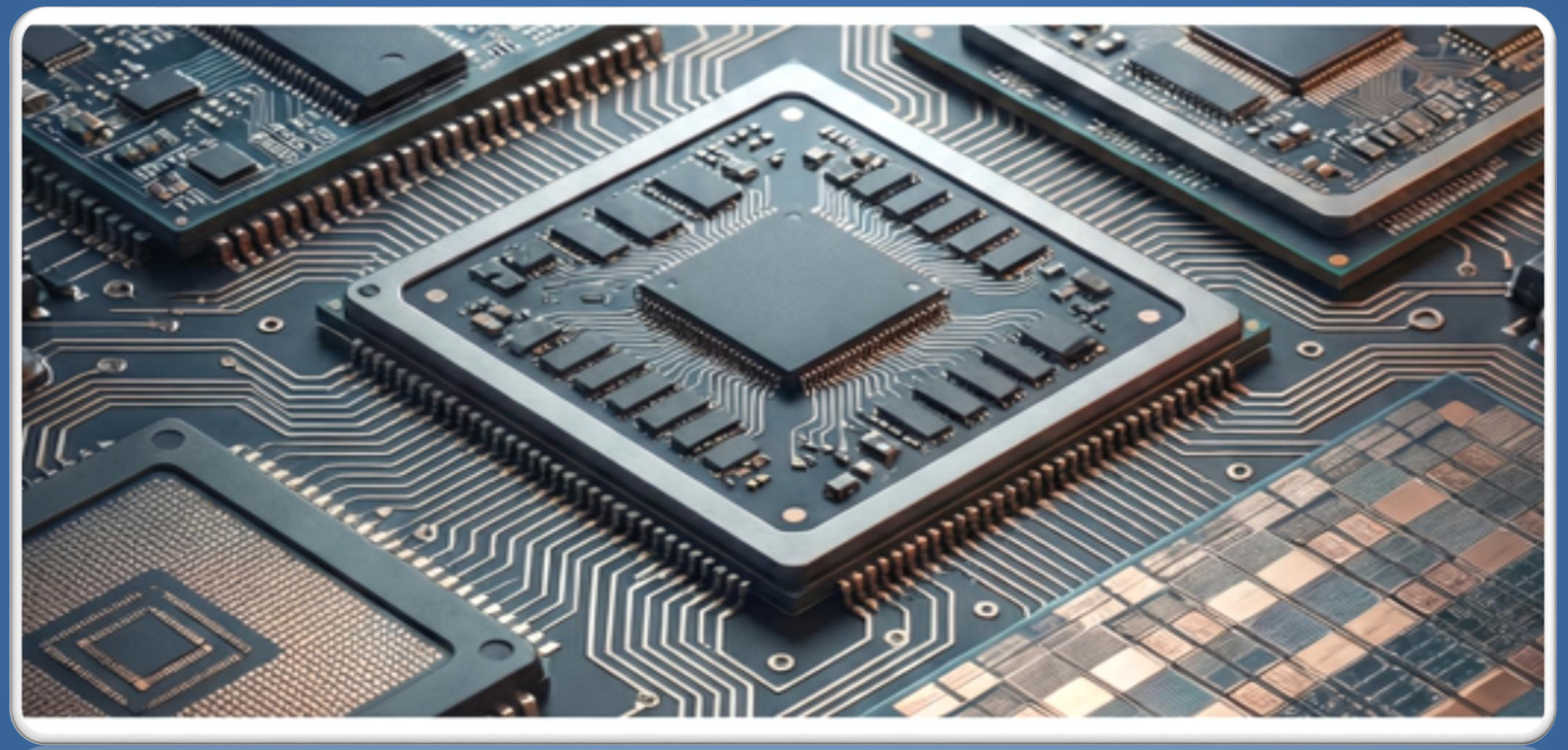
University of Boumerdes
Faculty of Technology
Department of Electrical Engineering Systems

Chapter I



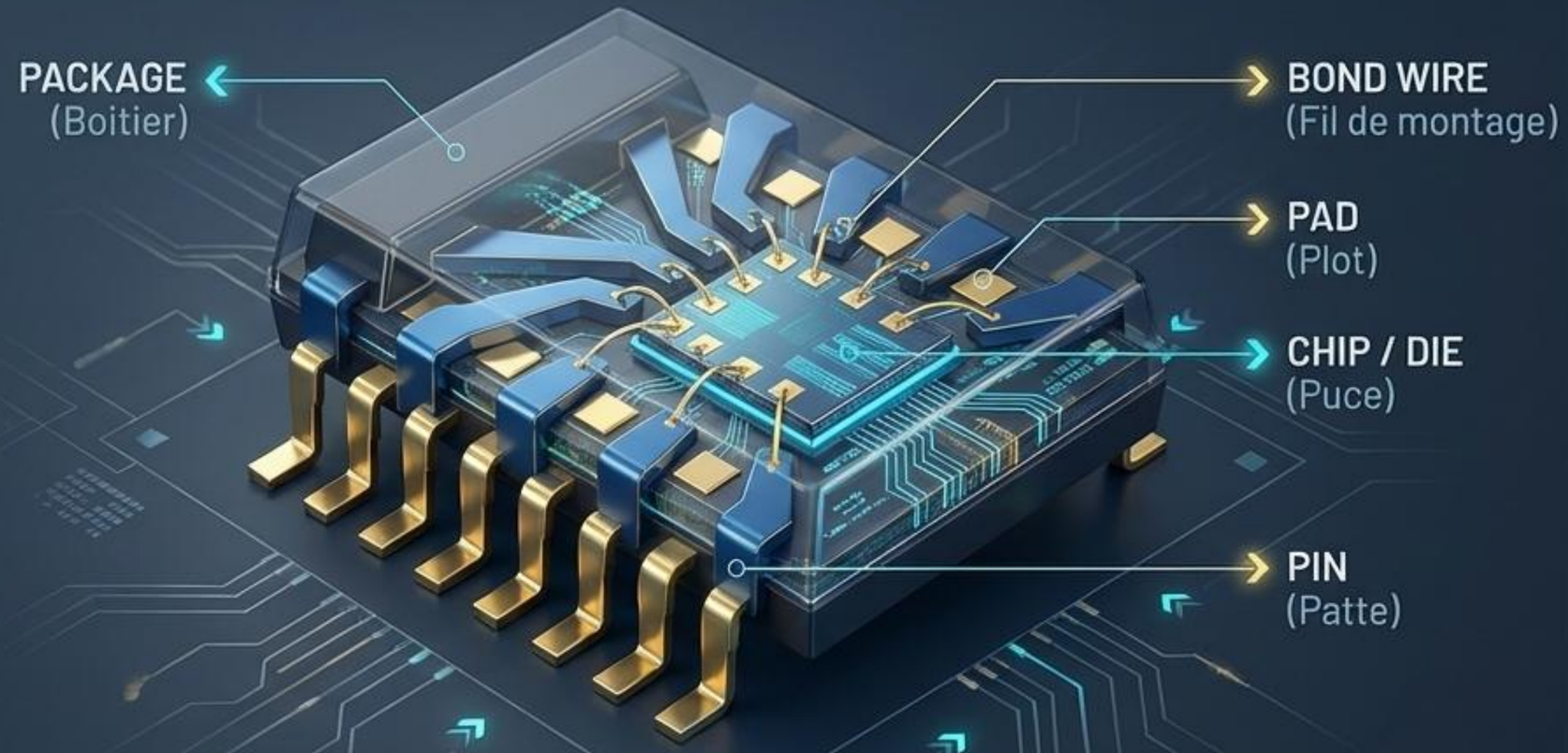
Digital Integrated Circuit Design Methodology

Mrs H. BOUMERIDJA

Course Outline

1. **Introduction**
2. **Digital Integrated Circuit Design Methodology:** The Top-Down Paradigm
3. **ASIC and FPGA Design Flows:**
    * Logic Synthesis
    * Placement and Routing
    * Functional Simulation and Verification
    * Hardware Programming and Implementation
4. **Implementation Techniques for Digital Integrated Circuits**

Digital Integrated Circuit Design Methodology and Implementation



A comprehensive guide to modern VLSI engineering, from abstract behavioral specifications to physical silicon layouts.

The Physical Foundations of an **Integrated Circuit**

What is an Integrated Circuit?

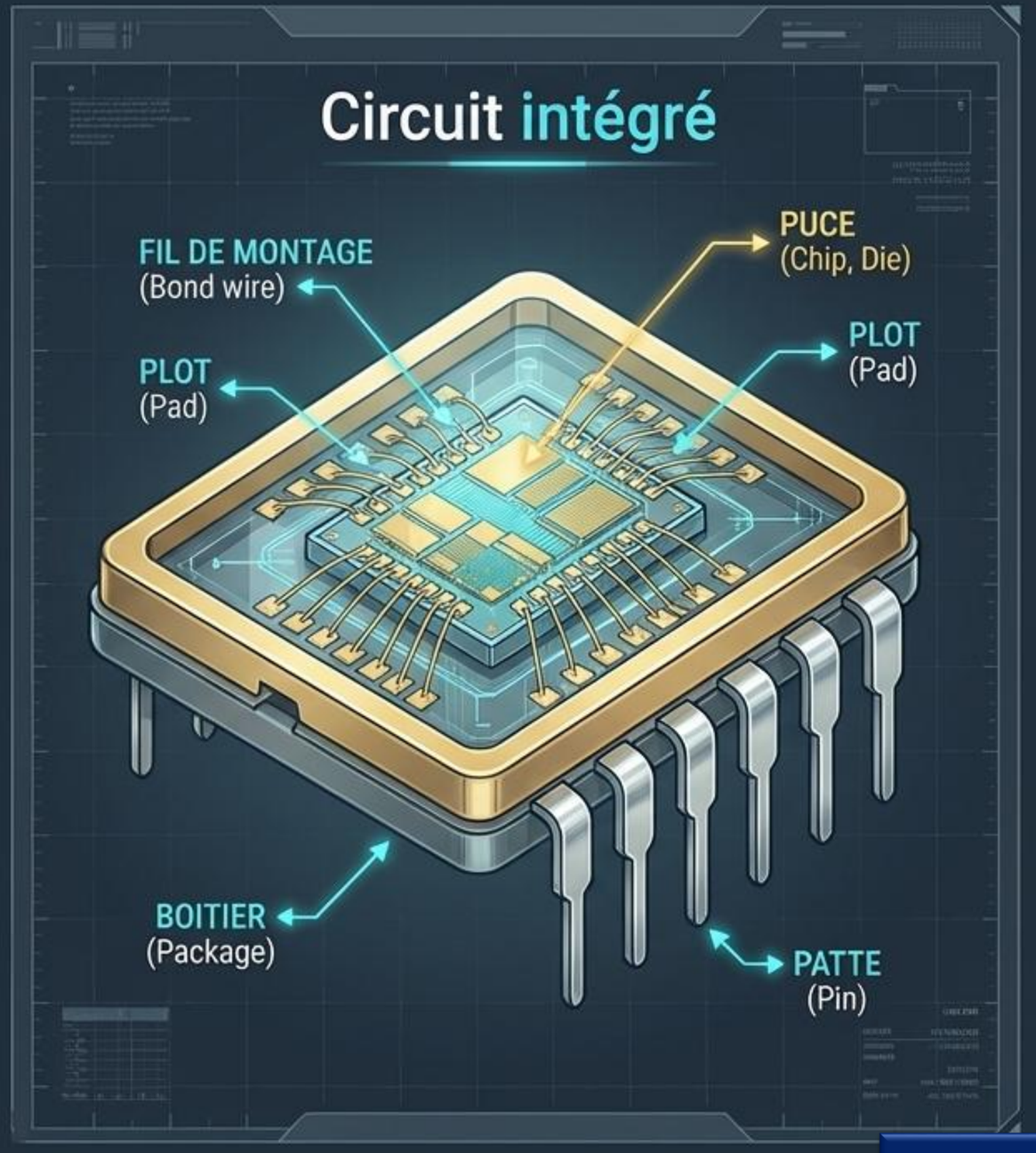
A microcircuit electronic implementation on a semiconductor substrate, typically Silicon.

Fundamental Components

- **Transistors** → Active semiconductor devices operating as switches or amplifiers.
- **Connections** → Metallic or polysilicon pathways interconnecting transistors to form complex networks.

Governance

Strictly defined by a specific technological process determining physical limits, performance boundaries, and die density.



The Chemical Masterpiece of Silicon Manufacturing

1. Oxidation

Growing a layer of silicon dioxide on the wafer surface to act as a pure insulator.

2. Lithography

Transferring circuit patterns onto the wafer surface using light-sensitive chemicals.

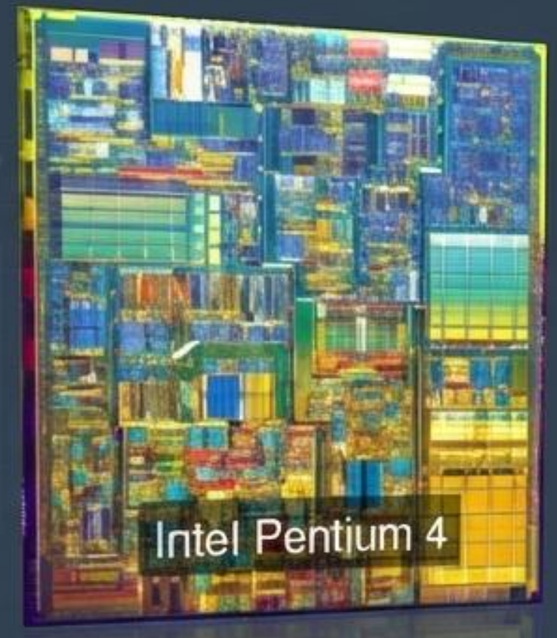
3. Etching

Selective chemical removal of material to define the physical boundaries of components.

The Critical Role of the Mask

At each stage, a mask acts as an absolute stencil. It ensures chemical processes (etching, doping) are applied only to predetermined microscopic areas.

The Relentless Momentum of Moore's Law



The Exponential Leap (1971 vs. 2001)

Intel 4004
2,300 Transistors
108 kHz Frequency
10.00 µm Technology

Intel Pentium 4
42,000,000 Transistors
2.0 GHz Frequency
0.13 µm Technology

Modern Design Friction Demands Strict Methodology

Massive Scale

Integrating hundreds of millions of fragile transistors without a single physical or logical error.

Gigacycle Frequencies

Managing signal integrity and precise timing margins at extreme GHz speeds.

Electronic Design Automation (EDA)

Power Dissipation

Containing strict thermal envelopes and preserving battery life in dense architectures.

Time to Market

Relentless commercial pressure to transition from abstract concept to silicon die in months.

Conclusion: Manual circuit design is obsolete. Systematic, rigorous methodologies are mandatory for survival.

Divide and Conquer Through Successive Refinement

The Top-Down Approach

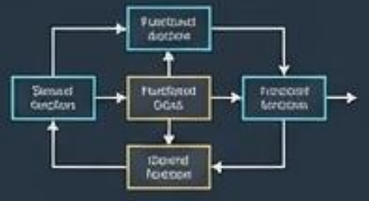
1. The "What" → The initial Specifications document defines system functions and operational execution conditions.
2. The "How" → Through architectural, logical, and geometric refinement, the "what" is mathematically transformed into physical transistors.

Optimized Flow

Uniquely suited for flexible implementations using standard cells or gate arrays.

The Four Cascading Levels of Design Abstraction

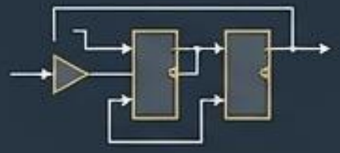
Level 1: Architectural



Description: High-level structural representation using functional blocks.

Tools: C/C++, FSMs, behavioral VHDL.

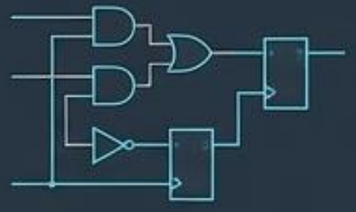
Level 2: Register Transfer Level (RTL)



Description: Structural components modeling data transfers between internal registers.

Action: Identifies exact hardware operations executing system specifications.

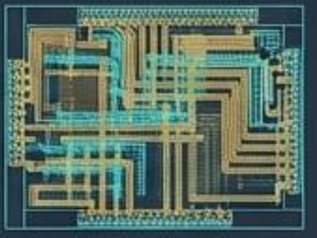
Level 3: Logic Level



Description: Circuit construction utilizing strict logic gates and flip-flops.

Tools: Bit-level operations via Truth Tables or State Tables.

Level 4: Geometric Level



Description: The final physical mask drawings dependent on the implementation technology.

Action: Cell realization, precise placement, and detailed routing.

Flow Steps 1 & 2: Abstract Description to Structural Synthesis

Step 1: Description and Modeling

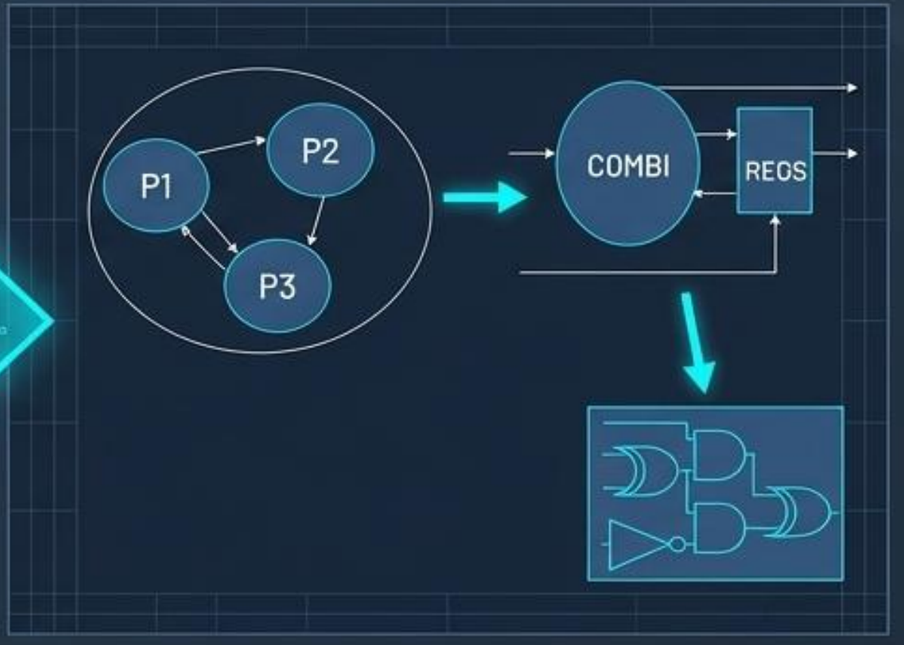
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE ieee.numeric_std.ALL;

ENTITY compteur_gen IS
  PORT ( h, compter, raz : IN std_logic;;
         sortie :  OUT std_logic_vector(Nb_bits-1 DOWNTO 0);
         retenne :  OUT std_legic;
-------------------------------------------------------
ARCHITECTURE synchrone OF compteur_gen IS
    SIGNAL s  : unsigned(Nb_bits-1 DOWNTO 0);
BEGIN
  P1 :PROCESS
    VARIABLE c : natural range 0 TO Modulo -1;
  BEGIN
-- description entierement synchrone
    WAIT UNTIL RISING_EDGE(h);
    IF raz = '1' THEN
      = :=0;
```

Translating client specifications into a Hardware Description Language (VHDL, Verilog, ABEL).

Synthesis Tool Constraints (Speed & Area)

Step 2: Compilation and Synthesis



The critical transformation of the HDL description into a structural Netlist of logic gates, mapped using specific target FPGA primitives.

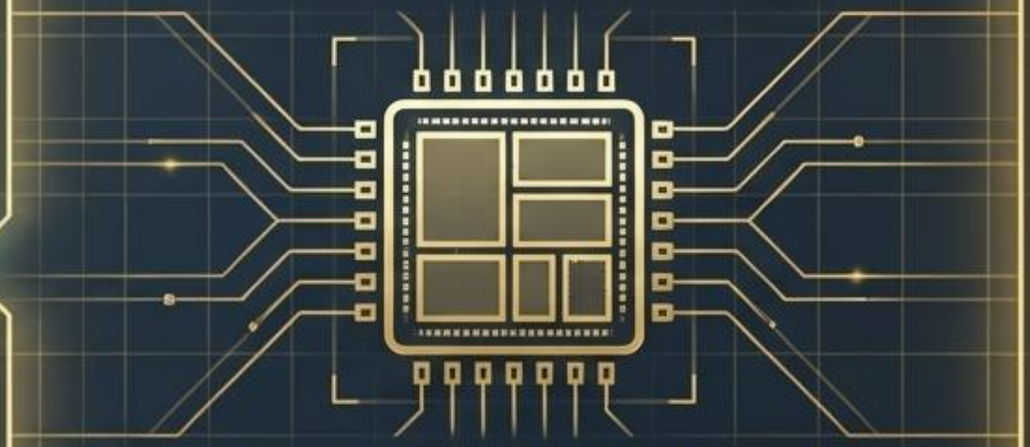
Flow Steps 3 & 4: Functional Verification and Spatial Floorplanning

Step 3: Functional Simulation

The Pre-Synthesis Checkpoint.

Validating the exact mathematical behavior of the code against original specifications before committing to hardware structures.

Step 4: Floorplanning

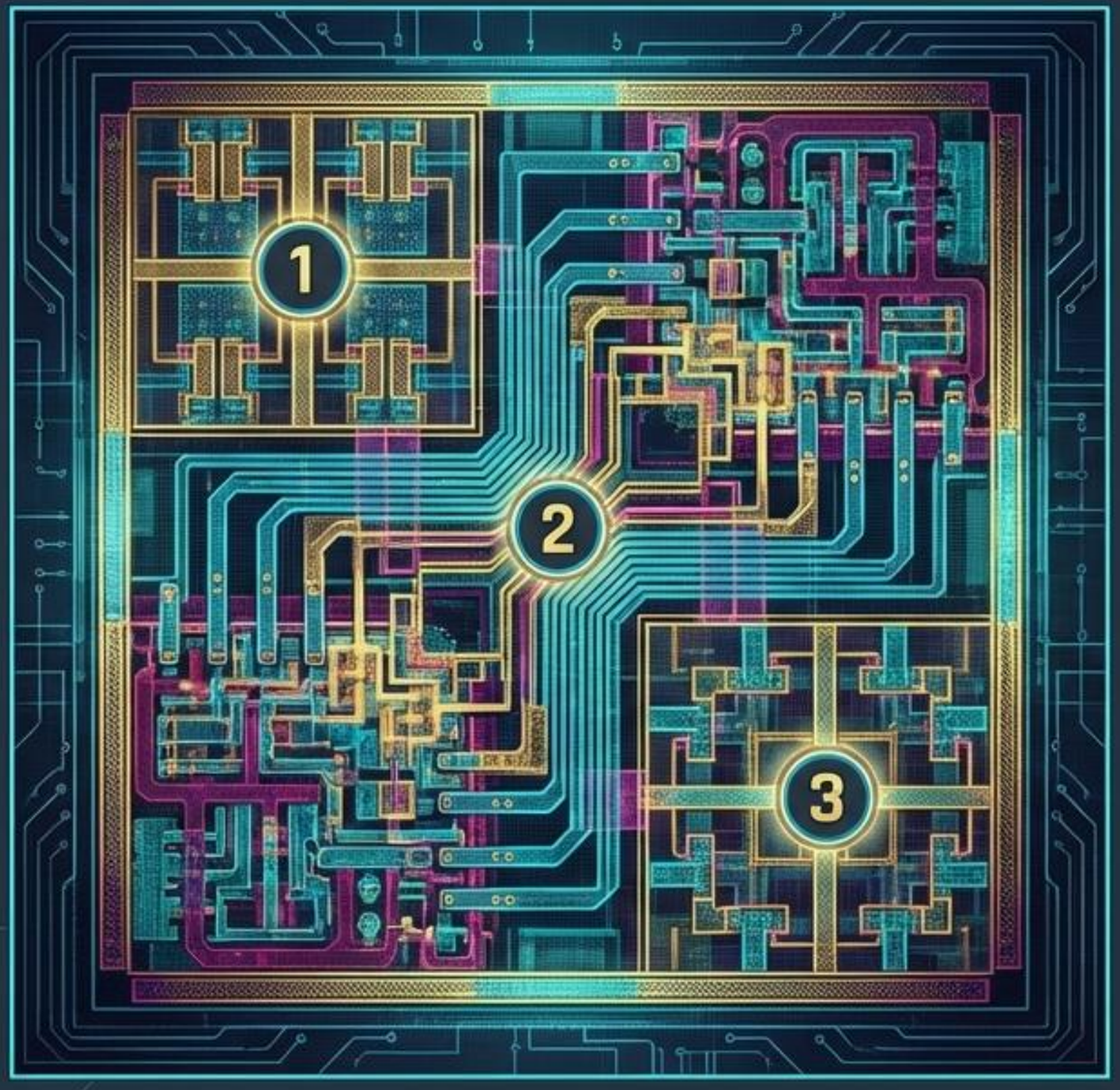


The architectural transition to physical space.

Establishes a mass plan, manages I/O constraints, and defines functional rows for cell placement.

Engineering Reality: The designer must strategically leave sufficient empty space between blocks strictly for signal routing, or risk catastrophic physical congestion.

Flow Step 5: The Physical Implementation



The Compilation of the Circuit

- **Placement**
  Positioning specific physical cells precisely according to the floorplan mass plan.
- **Routing**
  Global Routing: Defining general physical paths between cells.
  Detailed Routing: Drawing the exact, micro-level interconnections.
- **Clock and Power**
  Dedicated distribution networks for absolute signal integrity.
- **Back-Annotation**
  The critical extraction of true physical delays from routing paths, fed back into the netlist for post-layout accuracy.

Flow Step 6: Configuration and the User Constraints File

The Culmination of the ASIC/FPGA Pipeline

The physical implementation is locked, generating the final programming files.

The User Constraints File (UCF)

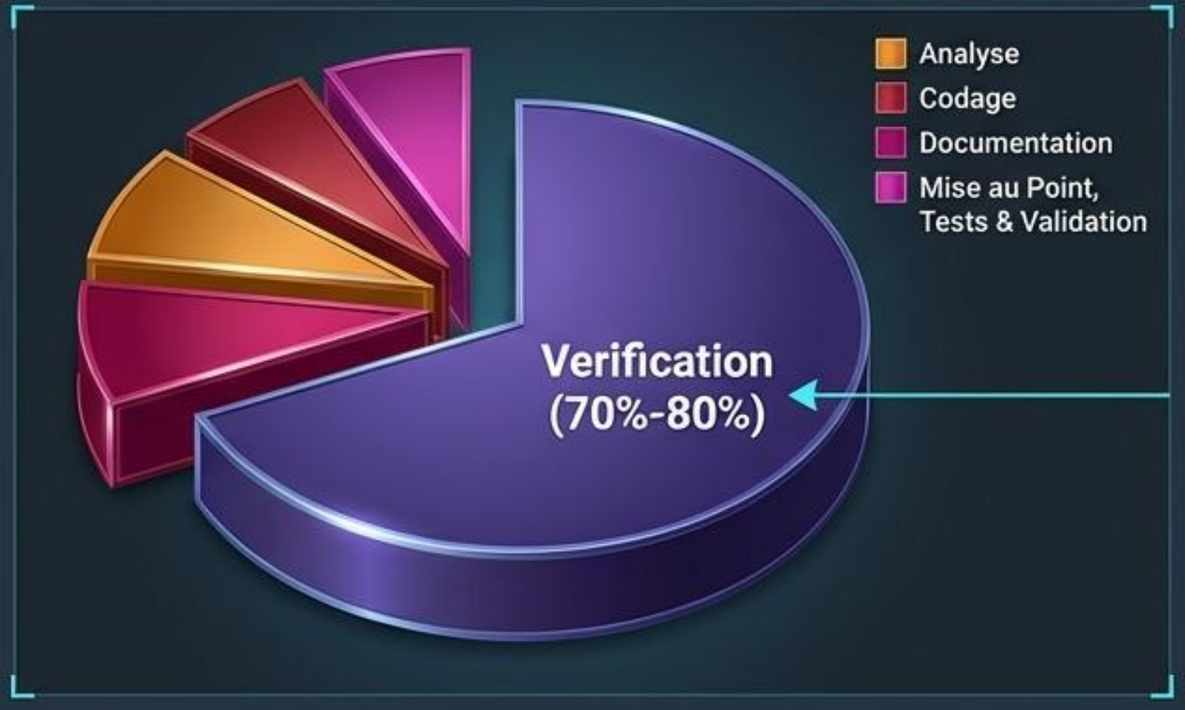
Physical Pin Placement

Explicitly mapping internal logical ports to the physical external pins of the IC package.

Timing Maximums

Locking in maximum allowable frequencies and signal delays to ensure the chip interfaces correctly with external systems.

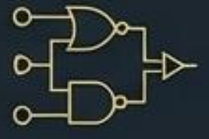
The Dominant Burden of System Verification



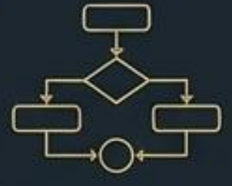
Verification consumes **70% to 80%** of the total design timeline.

The ultimate objective is proving the module will function **flawlessly** in its final, **integrated environment**.

Functional Simulation



Performed early. Proves the logic works purely as mathematics without physical bounds.



Timing Simulation

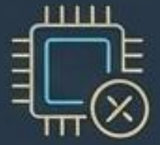
Performed post-layout. Uses back-annotated physical delays to prove the circuit survives real-world physics.

Proving Speed Without Simulation: Static Timing Analysis

```
Timing report:
+-------------+--------+------+-----------+-------------+
| Clock Net   | Resource| Fanout|Net Skew(ns)|Max Delay(ns)|
+-------------+--------+------+-----------+-------------+
| clk_BUFGP   | Global |   263 |      0.348 |       0.809 |
+-------------+--------+------+-----------+-------------+
Minimum period: 14.031ns (Maximum Frequency: 71.271MHz)
Minimum input arrival time before clock: 14.121ns
Maximum output required time after clock: 10.678ns
Maximum combinational path delay: 12.153ns

Area report:
Selected Device : 2s600efg676-6
Number of Slices:              315 out of  6912   4%
Number of Slice Flip Flops:    358 out of 13824   2%
Number of 4 input LUTs:        568 out of 13824   4%
Number of bonded IOBs:          50 out of   514   9%
Number of BRAMs:                 2 out of    72   2%
Number of GCLKs:                 1 out of     4  25%
```

The Limitation of Dynamic Simulation



Requires test vectors, making it impossible to computationally test every state in a chip with millions of transistors.

The Static Timing Analysis (STA) Solution

Calculates maximum operating speeds and verifies all setup and hold times across the network using topological mathematics.

The Result

Guarantees performance without executing a single simulation vector, operating as a rigorous mathematical proof of the physical layout's timing integrity.

The Tripartite Role of Hardware Description Languages

Specification

Utilized alongside simulators to define and lock down strict system requirements before any design begins.

Verification

Serves as the rigid testbench environment to validate the design logic under extreme simulated conditions.

Description

Operates with synthesis tools to define the exact physical hardware components, from full systems down to solitary logic gates.

VHDL is not merely software code; it is a multi-dimensional hardware modeling framework.

Validated Silicon Ready for the Market

- The Top-Down methodology and the 6-step flow guarantee that abstract whiteboard specifications successfully survive the journey into geometric reality.

- From billions of theoretical logic states to a fully verified, timing-accurate netlist, the resulting FPGA or ASIC is successfully configured.

The final product is a physical execution of Moore's Law, engineered to overcome power, speed, and scale barriers